Lab Assignment
Implement AMBA AHB Lite “Junior” Bus Master

Module Block Diagram:

Input/Output Signal Ports:
HRESETn: Active Low global reset of master
HCLK: Clock signal which times all bus transfers
ADDR: Requested address by the processor (provided by the test bench)
HWRITE: High for write transfer and Low for read transfer
HWDATA: Write data from the bus master to the slave
HRDATA: Read data from the bus slave
HREADY: Indicate whether the slave is ready to complete the current transfer
HADDR: 32-bit bus address
WRITE: Write request from the processor (provided by the test bench)
WDATA: Write data from the processor (provided by the test bench)
RDATA: Read data to the processor (outputted to the test bench)
### Example operations:

Please refer to the original AMBA 3 AHB-Lite Protocol for timing diagrams on Read and Write transfers with wait state.

1. **Reset:** (Takes 1 clock cycle)
   - Giving active low (0) to HRESETn should reset the MASTER by setting the values of all its output ports to 0’s. (HWRITE, HWDATA & HADDR)

2. **Read with no wait state:** (Lasts 2 clock cycles)
   - WRITE flag is set to zero
   - HREADY is high
   - At a positive clock edge ADDR data to be passed to HADDR
   - At the next clock cycle data available to read (HREAD) should be transferred onto the internal register called RDATA

![Example read transfer screenshot in simulation](image1)

3. **Write with no wait state:** (2 clock cycles)
   - WRITE flag is set high
   - HREADY high
   - At a positive clock edge ADDR data to be passed to HADDR
   - At the next clock cycle data available to write (WDATA) should be transferred onto the output bus HWDATA

![Example write transfer screenshot in simulation](image2)
Assignment:

- Implement simplified AMBA AHB-Lite “Junior” bus master in Verilog or VHDL. Write your own codes for the module. Use the standard test bench provided to test it.
- (Optional) Write your own test bench to improve the test coverage.
- Report your timing diagrams (screenshots) plotted in dve tool.
- Submit your report along with your codes before due date (09/22).

Note: Sample Verilog test bench code is available online. If you are writing your own test bench code, please comment on the cases you are considering in the report. Also please mention your comments on the code using “/* …<comment>… */” or “//”

Test cases used in the test bench:

1. reset
2. 2 continuous write
3. 2 continuous read
4. Write followed by read
5. Read and wait state (2 cycles)
6. Write and wait state (2 cycles)

Test bench file for Verilog is available here. (https://wustl.box.com/MyMastertb)