Lecture 4
3D Packaging and Integration

Xuan ‘Silvia’ Zhang
Washington University in St. Louis

ESE 566A: Modern System-on-Chip Design
ese.wustl.edu/~xuan.zhang/ese566
Previously on ESE 566A:
Diverse memory technology

source: Onur Mutlu, CMU
Acknowledgement

CPMT Distinguish Lecture
John H. Lau
ASM Pacific Technology
Mass Production

Commercia-
lization

Applied R&D

Basic/ Applied R&D

Don't use TSV

3D IC Packaging

Full swing production for memories.

Use TSV technology

3D IC Integration

Volume production for mobile products.

3D Si Integration

Active applied R&D is undertaken by Research Institutes. TSV cost is the key. In the phase of industrialization.

Die Stacking with wire bonds

Package on Package (PoP) Stacking

C2C, C2W, W2W Stacking

Still in upstream research, technological challenges such as KGD, yield & device architecture and EDA are key issues.

W2W Stacking
3D Packaging (No TSV)

3D/2.5D Integration

3D Challenges
3D IC Packaging

- Memory stacked with wirebonds
- Solder bumped flip chip assembly
- Package-on-Package (PoP)
- Chip-to-Chip interconnects
- Embedded fan-out wafer level package (eWLP)
Memory Stacked with Wirebonds

Samsung’s 8-Stack in iPhone 4s

Amkor’s Packaging with Cu Wires
PoP inside iPhone 6 Plus

Elpida's 1GB LPDDR3 (EDF8164A3PM-GD-F)

Package Substrate for LPDDR3

Package Substrate for A8 processor

Apple's application processor (POXY99001)

Top-side of the bottom PoP (426-ball)
Stacked Silicon Module

Heat spreader/sink (optional)

Microbump

Mother Chip

Daughter Chip

Solder Bump

Rigid or Flex Substrate

Solder Ball

PCB

Chip-to-Chip and Face-to-Face

Amkor’s POSSUM™ Assembly
Amkor’s Double POSSUM™ Configuration

Daughter Die

Grandma Die

PCB

Cu Pillar Micro-bumps with SnAg solder caps

Mother Die

POSSUM™ for Altera’s FPGA and ASIC

Outline

3D Packaging (No TSV)

3D/2.5D Integration

3D Challenges
Market Drivers for 3D IC

Performance driven
- "Mid term" driver: > 2010
  - Co-integration of RF + logic + memory + sensors in a reduced space

Electrical performance
- Interconnect speed and reduced parasitic power consumption

Cost driven
- "Long term" driver: > 2012

Form factor driven
- "Short term" driver: > 2008
  - Achieving the highest capacity / volume ratio

3D vs. "More Moore"
- Can 3D be cheaper than going to the next lithography node?

"More than Moore" Heterogeneous integration

Source: "3D IC & TSV Report", Tole Development

source: Joungho Kim, KAIST
Disadvantages of Stacked Chip with Wirebonds

- Long Interconnection
  - Long RC Delays
  - High Impedance for Power Distribution Network
  - High Power Consumption
  - Poor Heat Dissipation (Thick Substrate)

- Bonding Wire located in Chip Perimeter
  - Low Density Chip Wiring
  - Limited Number of I/O
  - Limited I/O Pitch
  - Large Area Package

- Complex Interposer
  - Long Redistribution Interconnection
  - Bonding Wire located in Interposer Periphery

source: Joungho Kim, KAIST
Advantages Offered by TSV

- Short Interconnection
  - Reduced RC Delays
  - Low Impedance for Power Distribution Network
  - Low Power Consumption
  - Heat Dissipation Through Via

- No Space Limitation for Interconnection
  - High Density Chip Wiring
  - No Limitation of I/O Number
  - No Limitation of I/O Pitch
  - Small Area Package

source: Joungho Kim, KAIST
Why does TSV Family happy ^_^?

Happy TSV Family:
- So fast! 🎶
- It's awesome!!

Sad Wire-bonding Family:
- So tired T^T!
- It takes too much energy !!

- Shorter distance!
- Lower loss of energy!

Elevator vs Stairs:
1st Floor
2nd Floor
3rd Floor
4th Floor
Through-Silicon Via (TSV)
Shortened Chip-to-Chip Interconnect

A four stack wire-bonded die package

Wirebonds are replaced by TSVs

Wire → TSV

Microbumps

Thin chips

Advantages:
- Smaller form-factor
- Low power consumption
- Wider bandwidth
- Better performance

Lau, Reliability of 3D IC Interconnects, 2011
Potential 3D Integration Applications

Memory-Chip Stacking
- DRAM or NAND Flash stacking with TSVs on organic substrate
- Over molding the DRAMs or NAND Flash

Wide I/O DRAM (Hybrid Memory Cube)
- DRAM stacking with TSVs on Logic Controller with TSVs
- Over molding the DRAMs

Wide I/O Interface (2.5D IC Integration)
- TSV-less chips on a device-less wafer (interposer) with TSVs
- Underfill is needed between chips and the interposer
Memory Stacking

- TSV Through Memory
  - enlarge memory capacity
  - lower power consumption
  - increase bandwidth
  - lower latency
  - reduce form factor
Samsung Flash and DRAM

- **16Gb Flash Memory**
  - 8 x 2Gb, 560µm thick

- **64GB DDR4 DRAM**
  - 16 x 4Gb, 20nm process with TSV
  - 2x fast, and 50% power
  - used in server farm
Hybrid Memory Cube (HMC)

- HMC Consortium
  - 8 members
  - SPEC published in 2013
  - adopted by HPC, networking, energy, wireless communication, transportation, security, high-end servers
HMC Architecture

- Divided into 16 Cores
- Logic Base at the Bottom
- 15x Performance, 70% Energy Per Bit
Altera’s Stratix FPGA with Micron HMC

Stratix V FPGA

10/100/1000 Ethernet Connectors

ATX Form Factor

Hybrid Memory Cube (HMC)

ATX Power Supply Connector

By providing equivalent bandwidth of greater than eight (8) DDR4-2400 DIMMs using a single HMC device.

Intel’s “Knight’s Landing”  

Fujitsu’s Tofu2

Wide I/O DRAM and High Bandwidth Memory (HBM)

HBM is designed to support bandwidth from 128GB/s to 256GB/s
2.5D Integration with Interposers

- Underfill
- UBM
- Cu Pillar
- Solder
- RDLs (Redistribution layers)
- TSV
- Interposer
- Package Substrate
- Build-up Layers
- Not-to-scale

Si

RDLs for lateral communications
Virtex-7 HT (Xilinx and TSMC) and Passive Interposers
Xilinx/TSMC’s 2.5D Integration:
Fine-pitch, high-I/O, high-performance, high-density

- Interposer
- C4 Bumps
- Devices (Cannot see)
- Metal Layers
- Metal Contacts
- 4RDLs: 0.4μm-pitch line width and spacing
- Each FPGA has >50,000 μbumps on 45μm pitch
- Interposer is supporting >200,000 μbumps

The package substrate is at least (5-2-5)
3D MEMS and IC:
Avago’s Film Bulk Acoustic Resonator (FBAR) with TSV
FBAR Hermetic Package and Bonding

(a) Cap Wafer

(b) FBAR Wafer

IC Cap Wafer

FBAR Wafer

Circuit
3D CMOS Image Sensor (CIS) Integration

- Front vs Back-Illuminated

- 2D vs 3D
Sony’s BI-CIS Integration

Backside illuminated CIS die

processing engine die

Pixel array

Logic circuits

Comparators

TSVs

Row drivers

Load Tr.'s

TSVs

Row decoders

Counters

Analog & Others
Outline

3D Packaging (No TSV)

3D/2.5D Integration

3D Challenges
EDA Solution for 3D

source: STM, DAC 2009
3D (TSV) Design Flow

source: R. Maheshwary, Synopsys
3D Test Strategies

- **Challenges**
  - stack testing (efficiency & cost)
  - low pin count test

- **Solutions**
  - test one die at a time with isolation logic
  - 1000x test compression at low pin cost
  - inter-die testing methodology
  - extend IEEE test standards
3D Thermal Considerations

- Challenges
  - multiple heat source (stack)
  - substrate thinning yields poor heat dissipation
  - elevated thermal gradient in 3D
  - => reliability and timing
Questions?

Comments?

Discussion?
After-Class Reading

- Learn more on the manufacturing process involved in 3D integration
  - face-to-face, face-to-back bonding
  - TSV processing Via-First or Via-Last
Lab Tutorials

- Linux Lab Remote Login
- Synopsys VCS
  - Functional verification
  - Support Verilog and VHDL simulation
Lab Preparation

- **AMBA 3 AHB-Lite Protocol**
  - [http://www.eecs.umich.edu/courses/eecs373/reading/ARM_IHI0033A_AMBA_AHB-Lite_SPEC.pdf](http://www.eecs.umich.edu/courses/eecs373/reading/ARM_IHI0033A_AMBA_AHB-Lite_SPEC.pdf)